THE INVENTION CLAIMED IS:

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1. An apparatus adapted to multiplex debug signals of an integrated circuit, the apparatus comprising:

at least a first multiplexing circuit and a second multiplexing circuit, wherein:

the first multiplexing circuit is adapted to receive first debug signals from an integrated circuit and to selectively multiplex at least a first portion of the first debug signals onto a first bus; and

the second multiplexing circuit is adapted to receive second debug signals from the integrated circuit and to selectively multiplex at least a first portion of the second debug signals onto a second bus;

a logic circuit adapted to combine any debug signals of the first bus and any debug signals of the second bus onto a third bus; and

an output stage adapted to selectively output debug signals of the third bus.

2. The apparatus of claim 1 wherein the output stage comprises a third multiplexing circuit adapted to receive debug signals of the third bus and to selectively multiplex the debug signals onto a fourth bus.

3. The apparatus of claim 2 wherein the third multiplexing circuit comprises:

a multiplexer adapted to receive the debug signals of the third bus and to selectively multiplex the debug signals onto the fourth bus; and

a control register coupled to the multiplexer and adapted to control multiplexing of debug signals by the

multiplexer.

4. The apparatus of claim 3 further comprising:

at least a first latch set coupled to the third bus and adapted to latch debug signals from the third bus at a first clock frequency and to output the latched debug signals to the multiplexer.

5. The apparatus of claim 1 wherein the first, second and third buses are equally sized.

6. The apparatus of claim 1 wherein the logic circuit performs a bit-by-bit OR operation.

7. The apparatus of claim 1 wherein the first and second multiplexing circuits are adapted to multiplex on a nibble basis.

8. The apparatus of claim 1 wherein the first multiplexing circuit is part of a first partition of the integrated circuit adapted to selectively multiplex the first debug signals of the integrated circuit and wherein the second multiplexing circuit is part of a second partition of the integrated circuit adapted to selectively multiplex the second debug signals.

9. The apparatus of claim 8 wherein the first multiplexing circuit comprises:

a first multiplexer adapted to receive the first debug signals from the integrated circuit and to selectively multiplex at least the first portion of the

first debug signals; and

a first control register coupled to the first multiplexer and adapted to control multiplexing of the first debug signals by the first multiplexer; and

wherein the second multiplexing circuit comprises:

a second multiplexer adapted to receive the second debug signals from the integrated circuit and to selectively multiplex at least the first portion of the second debug signals; and

a second control register coupled to the second multiplexer and adapted to control multiplexing of the second debug signals by the second multiplexer.

10. The apparatus of claim 9 further comprising:

a first latch set coupled to the first multiplexer and adapted to latch debug signals output by the first multiplexer at a first clock frequency; and

a second latch set coupled to the second multiplexer and adapted to latch debug signals output by the second multiplexer at a second clock frequency.

11. The apparatus of claim 1 wherein the first and second multiplexing circuits are part of a single partition of the integrated circuit adapted to selectively multiplex the first and second debug signals.

12. The apparatus of claim 11 wherein the first multiplexing circuit comprises:

a first multiplexer adapted to receive the first debug signals from the integrated circuit and to

selectively multiplex at least the first portion of the first debug signals; and

a first control register coupled to the first multiplexer and adapted to control multiplexing of the first debug signals by the first multiplexer; and

wherein the second multiplexing circuit comprises:

a second multiplexer adapted to receive the second debug signals from the integrated circuit and to selectively multiplex at least the first portion of the second debug signals; and

a second control register coupled to the second multiplexer and adapted to control multiplexing of the second debug signals by the second multiplexer.

13. The apparatus of claim 12 further comprising:

a first latch set coupled to the first multiplexer and adapted to latch debug signals output by the first multiplexer at a first clock frequency; and

a second latch set coupled to the second multiplexer and adapted to latch debug signals output by the second multiplexer at a second clock frequency.

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14. An apparatus adapted to multiplex debug signals of an integrated circuit, the apparatus comprising:

at least a first multiplexing circuit and a second multiplexing circuit, wherein:

the first multiplexing circuit is adapted to receive first debug signals from an integrated circuit and to selectively multiplex at least a first portion of the first debug signals onto a first bus; and

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the second multiplexing circuit is adapted to receive second debug signals from the integrated circuit and to selectively multiplex at least a first portion of the second debug signals onto a second bus;

a logic circuit adapted to combine any debug signals of the first bus and any debug signals of the second bus onto a third bus; and

a third multiplexing circuit adapted to receive debug signals of the third bus and to selectively multiplex the debug signals onto a fourth bus.

15. A method of multiplexing debug signals of an integrated circuit, the method comprising:

receiving first debug signals from an integrated circuit;

selectively multiplexing at least a first portion of the first debug signals onto a first bus;

receiving second debug signals from the integrated circuit;

selectively multiplexing at least a first portion of the second debug signals onto a second bus;

combining any debug signals of the first and second buses onto a third bus; and

selectively outputting debug signals of the third bus.

16. The method of claim 15 wherein selectively outputting debug signals of the third bus comprises selectively multiplexing the debug signals onto a fourth bus.

17. The method of claim 16 further comprising latching at least a portion of the debug signals of the third bus at one or more clock frequencies prior to selectively multiplexing the debug signals onto the fourth bus.

18. The method of claim 15 wherein the first, second and third buses are equally sized.

19. The method of claim 15 wherein combining any debug signals of the first and second buses onto a third bus comprises performing a bit-by-bit OR operation.

20. The method of claim 15 wherein selectively multiplexing is performed on a nibble basis.

21. The method of claim 15 wherein the step of selectively multiplexing at least a first portion of the first debug signals onto a first bus is performed by a first partition of the integrated circuit; and

wherein selectively multiplexing at least a first portion of the second debug signals onto a second bus is performed by a second partition of the integrated circuit.

22. The method of claim 21 further comprising:

latching the first portion of the first debug signals at a first clock frequency following multiplexing of the first portion of the first debug signals; and

latching the first portion of the second debug signals at a second clock frequency following

multiplexing of the first portion of the second debug signals.

sub A5 23. The method of claim 15 wherein the steps of selectively multiplexing at least a first portion of the first debug signals onto a first bus and selectively multiplexing at least a first portion of the second debug signals onto a second bus are performed by a single partition of the integrated circuit.

24. A method of multiplexing debug signals of an integrated circuit, the method comprising:

receiving first debug signals from an integrated circuit;

selectively multiplexing at least a first portion of the first debug signals onto a first bus;

receiving second debug signals from the integrated circuit;

selectively multiplexing at least a first portion of the second debug signals onto a second bus;

combining any debug signals of the first and second buses onto a third bus; and

selectively multiplexing the debug signals onto a fourth bus.

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